REMARKS

Claims 19-20, 22-26, 29-38, and 40-41 are Allowable

The Office has rejected claims 19-20 and 22-38, at paragraphs 5 and 6 of the Final Action, under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 5,956,493 ("Hewitt") in view of U.S. Patent No. 5,083,261 ("Wilkie"). Applicants respectfully traverse the rejections.

Independent Claim 19

None of the cited references, including Hewitt and Wilkie, disclose or suggest the specific combination of claim 19. For example, Hewitt and Wilkie do not disclose loading a timer resolution parameter into a control register, where the timer resolution parameter relates to an amount of time associated with a first counting cycle of a first counter timer and a second counting cycle of a second counter timer, as recited in claim 19. Further, Hewitt and Wilkie do not disclose dynamically adjusting a timer resolution parameter based on the activity level of a memory bus, as recited in claim 19. In contrast to claim 19, Hewitt discloses programming bus masters with an initial count value based on the latency requirements of each bus master. (*See* Hewitt, col. 5, ll. 50-62). Additionally, Hewitt discloses that the closer a count value is to a value of zero, the higher the priority level given by a bus arbitration control unit. (*See* Hewitt, col. 4, ll. 58-62). Hewitt does not disclose a timer resolution parameter, in addition to timer count values, where the timer resolution parameter relates to an amount of time associated with a first counting cycle of a first counter timer and a second counting cycle of a second counter timer, as recited in claim 19. Hewitt also does not disclose dynamically adjusting the timer resolution parameter based on the activity level of a memory bus, as recited in claim 19. Further, Wilkie does not disclose a timer resolution parameter that relates to an amount of time associated with a first counting cycle of a first counter timer and a second counting cycle of a second counter timer, as recited in claim 19. Wilkie also does not disclose dynamically adjusting the timer resolution parameter based on the activity level of a memory bus, as recited in claim 19. Hence, claim 19 is allowable.

Claims 20, 22-26, and 40-41 depend from claim 19, which Applicants have shown to be allowable. Hence, Hewitt and Wilkie fail to disclose at least one element of each of claims 20, 22-26, and 40-41. Accordingly, claims 20, 22-26, and 40-41 are also allowable, at least by virtue of their dependency from claim 19.

Further, the dependent claims include additional features not disclosed or suggested by Hewitt and Wilkie. For example, neither Hewitt nor Wilkie disclose or suggest loading a first timer resolution parameter and a second timer resolution parameter into a control register, where the first timer resolution parameter corresponds to an amount of activity by a first functional device on a system bus and the second timer resolution parameter corresponds to an amount of activity by a second functional device on the system bus, as recited in claim 41. For this additional reason, claim 41 is allowable.

Independent Claim 29

None of the cited references, including Hewitt and Wilkie, disclose or suggest the specific combination of claim 29. Neither Hewitt nor Wilkie disclose or suggest loading a timer resolution parameter into a control register, where the timer resolution parameter relates to an amount of time associated with a first counting cycle of a first counter timer and a second counting cycle of a second counter timer, as recited in claim 29. Further, Hewitt and Wilkie do not disclose or suggest dynamically adjusting the timer resolution parameter based on the activity level of a memory bus, as recited in claim 29. Hence, claim 29 is allowable.

Claims 30-38 depend from claim 29, which Applicants have shown to be allowable. Hence, Hewitt and Wilkie fail to disclose at least one element of each of claims 30-38. Accordingly, claims 30-38 are also allowable, at least by virtue of their dependency from claim 29.

There is no suggestion or motivation to make the asserted combination of Hewitt and Wilkie

Applicants submit that there is no suggestion or motivation to make the asserted combination of references either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Hewitt is directed to a bus arbitration control unit that compares the current count value of a number of counters to determine a bus master that has

priority to access a system bus. (*See* Hewitt, col. 4, ll. 54 – col. 5, ll. 13). Hewitt discloses that each bus master is associated with a respective counter and that the counters begin counting from a programmed initial count value. (*See* Hewitt, col. 5, ll. 50-62). Wilkie is directed to an interrupt priority circuit that intercepts signals by resources attempting to access a processor and provides the processor with a vector corresponding to the resource with the higher priority. Further, Wilkie discloses that the interrupt priority circuit allows a user to selectively override a pre-established priority scheme and dynamically define any one resource as having the highest priority. (*See* Wilkie, col. 3, ll. 5-14). Hewitt and Wilkie disclose implementing only one prioritization method at any given time, not both operations at the same time. Thus, combining the counter value prioritization system of Hewitt with the interrupt priority circuit of Wilkie would require substantial reconstruction of the elements shown in Hewitt, as well as a change in the basic principle under which Hewitt was designed to operate. Therefore, for this additional reason, the rejections of claims 19-20 and 22-38 over Hewitt and Wilkie are improper and should be withdrawn.

Claim 21 is Allowable

The Office has rejected claim 21, at paragraphs 7 and 8 of the Final Action, under 35 U.S.C. §103(a), as being unpatentable over Hewitt in view of Wilkie and further in view of what was well know in the art at the time of applicant's invention as evidenced by U.S. Patent No. 6,226,702 ("Yakashiro"). Applicants respectfully traverse the rejections. Claim 21 depends from claim 19, which Applicants have shown to be allowable. Yakashiro does not disclose or suggest the elements recited in claim 21 that are not disclosed or suggested by Hewitt and Wilkie. For example, Yakashiro does not disclose or suggest dynamically adjusting a timer resolution parameter based on the activity level of a memory bus, where the timer resolution parameter relates to an amount of time associated with a first counting cycle of a first counter timer and a second counting cycle of a second counter timer, as recited in claim 19. Thus, claim 21 is allowable at least by virtue of its dependency from claim 19.

CONCLUSION

Applicants have pointed out specific features of the claims not disclosed, suggested, or rendered obvious by the references applied in the Office Action. Accordingly, Applicants

respectfully request reconsideration and withdrawal of each of the rejections, as well as an indication of the allowability of each of the pending claims.

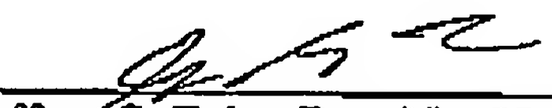
Any changes to the claims in this amendment, which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

6-6-2007
Date



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